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# SAL Storage for the AN/UPA-59/60 IFF Decoders



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13 ABSTRACT

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A modification of the existing decoders is proposed, consisting of a one-for-one replacement of a printed-circuit board within the main equipment. A feasibility model of the circuit-board replacement was constructed and tested in the NRL ground IFF system. This replacement board makes use of a new intergrated circuit, called the rubber shift register, which was developed under an NRL contract and represents the first known use of this component, The rubber shift register is a completely-variable-lenght shift register which has the ability to adapt its overall length to that of the incoming data on a real time basis.

Performance of SAL parity with the new circuit board has been demonstrated as being superior to the existing circuit board. Retrofit of existing equipment with new circuit boards to permit operation of the SAL parity function is recommended.

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| Altitude filtering | | | | | | |
| Variable shift register | | | | | | |
| AN/UPA-59/60 | | | | | | |
| SAL (Selected Altitude Layers) | | | | | | |

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## ABSTRACT

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Performance of SAL parity with the new circuit board has been demonstrated as being superior to the existing circuit board. Retrofit of existing equipment with new circuit boards to permit proper operation of the SAL parity function is recommended.


## PROBLEM STATUS

This is an interim report; work is continuing on other phases of the problem.

## AUTHORIZATION


NRL Problem 54R03-06.401
USMC (NAVELECSYSCOM) CP53-144-002-7638

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NAVELECSYSCOM S17-14-6220

# SAL STORAGE FOR THE AN/UPA-59/60 IFF DECODERS

G. P. Nelson

## BACKGROUND

The AN/UPA-59/60 IFF decoders can provide display of aircraft targets within an altitude layer selected by front panel switches. Determination of aircraft altitude in the decoder is done with the target's response to Mode C interrogations. Mode C is the civil and military altitude reporting mode. The decoder has two different types of SAL display, corresponding to different end uses and/or tactical situations.

The first type of display makes use of the received Mode C information only, i.e., a specific decoder is challenging and displaying Mode C only, although the overall IFF system may be interrogating other modes as requested by other decoders. The PPI display for this operation consists only of the Mode C bracket decodes of aircraft within the selected layer. This display permits the operator to observe and determine which aircraft are within the layer, excluding all others. In essence, the decoder is operating as an altitude filter. The primary usage of this display is in Air Traffic Control (ATC) functions, where other aircraft, those not in the layer, really represent undesirable clutter to the operator.

The second type of SAL display uses the responses from two different interrogation modes, one of which is Mode C. In this type of operation, the results of the non-Mode C interrogation are correlated against the results of the Mode C interrogation to determine the actual PPI display. The names SAL parity or SAL parity check are used to refer to this type of display. The PPI display in SAL parity operation is the passive decode of the non-Mode C interrogation response. If the target is not within the altitude layer, it is shown as a simple bracket decode. On the other hand, if the target is inside the altitude layer, the presentation is stretched in length (range), so that it appears brighter in intensity than the other targets. Operationally, SAL parity permits the PPI operator to perform a flight-following function, in which the aircraft's adherence to a prescribed altitude may be continually monitored.

Operation of the Navy's AN/UPA-59 decoder and the Marine Corp's AN/UPA-60 decoder showed serious deficiencies in SAL parity operation. The deficiencies have generally not been reported on previously and were found when the decoders were used with NRL's operational IFF system. Work to find the causes behind the deficiencies and determine corrective action was pursued under NRL Problems 57R03-02 (NAVELEX) and 57R03-06 (USMC). Since the two decoders are electrically identical, differing only in mechanical configuration and environmental performance requirements, the results of the work are equally applicable to both equipments.

The work being reported on is the result of several different tasks assigned to NRL. NAVELEX Problem X1714-1222 called for a study of AIMS interface requirements and reporting on possible improvements. It was under this assignment that the original deficiencies were discovered. NAVELEX Problem X1714-1223 called for studies of synchronization techniques to varying PRFs. A specialized integrated circuit, the rubber shift register,was developed under this problem. Corrective action to SAL parity requires similar techniques to those of the rubber shift register. A demonstration circuit board of a SAL parity modification was constructed using 24 rubber shift registers, and represents the first known application of this component to practical systems.

## SYSTEM INTERFACE PROBLEMS

The performance deficiencies noted with SAL parity operation were either no parity display whatsoever, or extremely erratic and intermittent operation. When a SAL parity display was obtained, the PPI presentation was noted to be that of a very broken target. Since operation of the other type of SAL display, using Mode C only, was satisfactory, investigation of the deficiencies was concentrated in one area, the SAL memory circuitry.

Performance of the SAL parity function requires that the decoder determine, during the Mode C receiver gate period, all aircraft which are within the altitude layer. This information, including the range of those aircraft, must be stored in some type of memory, otherwise known as SAL store. The information contained in memory is read out and correlated with the other, non-Mode C, mode during that mode's receiver gate period.

The decoder specifications, MIL-D-28736(EC) for the Navy's AN/UPA-59 and MIL-D-28755(EC) for the Marine Corps' AN/UPA-60,requires that SAL storage provide a range resolution of $\pm$ 0.4 nautical mile while providing for continuous ranging to a maximum of 350 nautical miles without additional operation of manual controls. The specifications further imply, but do not state as such, that the decoders be capable of normal operation when installed in a typical IFF system. It is these specifications, both stated and implied, that the present equipment is incapable of meeting.

Investigation of the problems revealed three reasons why the present SAL parity feature does not work properly. These reasons are:

1. The basic SAL memory can not accommodate differing interrogation rates and receiver gate lengths without adjustment of the internal operating and set-up controls.

2. The SAL memory circuitry was not designed to take into account typical system interrogation interlace patterns and sequences.

3. Improper design and design techniques were incorporated throughout the SAL store printed circuit board.

INTERROGATION RATES

The equipment's contractor, Cardion Electronics, decided to use a long shift register as the basic SAL memory. The apparent reasons behind this decision were that in operation the memory functions as a serial read in, serial read out device. If a constant clock frequency is used to drive the register, target range is stored within the register by the bit location in the register. Although there is nothing inherently wrong with use of a shift register in this application, the design did not take into account operation with differing system interrogation rates or receiver gate periods.

The inability of the decoder to accommodate differing interrogation rates and receiver gate lengths is in direct violation of specification requirements. The specification states that the decoder shall "Provide for continuous ranging to a maximum range of 350 nautical miles without additional operation of manual controls". In contrast to the specification, the SAL store circuit board has the following adjustments, which must be set to the particular IFF system used with the decoder:

1. A 4-position link adjustment, labeled coarse range select, which fixes the number of bits used in the long shift register forming the basic SAL memory.

2. Three 2-position link adjustments, labeled fine range select, which add or subtract capacitance from the clock oscillator circuit, thus changing the effective shift register length.

3. A variable capacitor, also part of the fine range select, to set the clock oscillator to the exact frequency required by the system.

The actual SAL storage in the decoder is a long shift register containing up to 500 individual flip-flops or bits of storage. Information in the form of Code C SAL decodes is read into the register memory during the Mode C receiver gate period. The stored information is read out of the register during the parity mode receiver gate period. Since the register clock is started immediately after interrogation and continues for the receiver gate duration, the effective range of the target is stored by location of the information bit in the register.

Because SAL decodes are stored in the register in range ordered sequence and must be correlated with the results of later interrogation, achieving proper SAL parity operation requires information read out in identical sequence and at exact relative time to information read in. This is to say that a SAL decode occurring 1000 microseconds after a Mode C interrogation must be read out 1000 microseconds after parity mode interrogation, not 999 or 1001 microseconds. In the absence of additional synchronization, the fixed number of register bits and set clock frequency determine a single, fixed system range at which proper

operation is obtained. This fixed range is given by the equation,

$$R = \frac{N}{f\ (12.37)} \quad ,$$

where R is equal to the range, in nautical miles, N is equal to the number of register bits, and f is the clock oscillator frequency.

The present circuit board does contain circuitry to handle limited synchronization of small deviations from the ideal range. The method used is to load an extra pulse, called the Stop Pulse, into the register. However, the Stop Pulse is indistinguishable from that of a SAL decode so that if system range differs greatly from the set-up range, the Stop Pulse and actual SAL decodes become intermixed. When intermixing occurs, data read in and read out is not at the same relative time, preventing proper correlation of information, producing a functional failure of SAL parity operation.

This SAL parity failure shows up on the PPI display as no stretched targets, meaning that there are no apparent targets within that altitude layer. Erroneous information is being given to the PPI operator, without the operator being aware of it.

This functional failure renders the SAL parity feature almost worthless for most Navy and several Marine Crops decoder installations. Many ships are equipped with multiple search and tracking radars, each with its own IFF system. Due to the characteristics of individual radars, the associated IFF systems will have different PRFs and receiver gate durations. Selection of radar and IFF system is by the RADAR SELECT switch on the front panel of the PPI, and is at the operator's discretion. However, within the decoder, the SAL Store card can be set-up to match the characteristics of only one system, and must necessarily neglect the remaining. Also, it should be noted that the ships which would most be expected to utilize SAL parity operation, the carriers, the DLGs, all have multiple radar systems.

It is felt that the inability of the decoder to adequately display SAL parity information in a multiple system environment could definitely be categorized as that of a "latent defect" since it does not meet the stated specification requirements.

INTERROGATION INTERLACE PATTERNS

The decoders are not designed to adequately handle typical system interrogation interlace patterns. This occurs when interlace counts exceed a value of one, and worsens with increasing counts. All preproduction bench tests performed by NRL on the AN/UPA-60 decoder, both at the contractor's plant and at NRL, used an interrogation sequence with a count of one. A typical one count sequence would interrogate Mode 3, Mode C, 3, C, 3, C, etc. However, in actual

system operation, the interrogation sequence is dictated by requirements for proper defruiter operation, typically needing a count of four. An example of a fo· count interrogation sequence would be: Mode 3, 3, 3, 3, Mode C, C, C, C, 3, 3, 3, 3, C, etc.

Present SAL parity operation stores only the results of the latest Mode C interrogation, and destructively reads that information out of memory on the first parity mode interrogation. Applied to the four count example in the above paragraph, only the results of the Mode C interrogation immediately preceding the Mode 3 are stored. The information received from the three earlier Mode C interrogations is ignored. Assuming that Mode 3 is the parity mode, the stored SAL information is destructively read out of memory on the first Mode 3 interrogation in the sequence. The next three Mode 3 interrogations can not show parity since there is no longer any information in the SAL memory. Thus, from a total of eight interrogations, parity is determined only once, using only two of the eight interrogations.

Assuming that all interrogations are answered and decoded 100%, not a valid assumption but still useful for explanation, the effect on a PPI presentation ranges from a severe loss of apparent target brightness, as only one of every eight interrogations is shown, to a worst case of no display at all, such as can happen with an AN/SPA-25 indicator which time-shares the bearing cursor with the target sweep on a one-for-eight basis. Actual system operation shows the overall effect to be very pronounced since replies are never received and decoded 100%. A loss of a specific SAL decode or parity mode decode, whether due to transponder deadtime, prior defruiting operations, or the degarbling function, eliminates parity display for a minimum of sixteen interrogations. The display video loss is further increased by time shared PPI cursors. Actual viewing tests with live targets have shown the chances of having broken and/or missing target displays are greatly increased over normal operation without SAL. Figures 11 through 18 show some of this effect.

The fault for these two related problems probably lies equally between the equipment's prime contractor and the government. The equipment specifications do not contain any information as to either what the probable mode interlace sequence will be, or that there is an interlace count greater than one. Further, the specification almost rules out storing the results of more than the last Mode C interrogation, in spite of its desirability. The contractor, however, must assume some partial responsibility. From performance on prior contracts, a much-touted fact in original proposals, the contractor does have knowledge of interrogation mode sequences and actual system operating parameters. Knowingly producing an equipment with marginal or non-existant system performance, without attempting to inform the customer, does seem to be a questionable practice.

## CIRCUIT DESIGN DEFICIENCIES

The third problem area in the SAL store printed circuit board results from improper design practices. The clock oscillator, used to shift the SAL parity information through the register memory, does not have sufficient power supply decoupling to isolate it from other decoder circuits. The observed defect,

shown in the oscilloscope pictures of Figures 1 and 2, is a slight difference in oscillator frequency between the Mode C data read-in and the parity mode data read-out. Figure 1 shows the oscillator at turn-on, immediately after interrogation, for both Mode C and the parity mode. As can be seen from this picture, the turn-on points are essentially identical, with the oscillator wave forms exactly in phase during both modes. Figure 2 shows the same oscillator test point, but with the display delayed approximately equal to 200 nautical miles. As can be seen from the photograph, there is now a phase shift between modes equal to 0.5 microseconds. This is not desirable as the overall function of the circuitry is correlation between modes. Timing differences between modes does reduce correlation.

Another common design error is in the application of integrated circuits and the use of typical component values rather than worst case or guaranteed minimum/maximum values. The primary integrated circuits used by the contractor are the 5400/7400 series Transistor-Transistor Logic (TTL) originally introduced by Texas Instruments.

The TTL circuts are sometimes interconnected in a manner which can not guarantee the propagation of a logical "zero" state. Figure 3 illustrates a common mistake which is repeated four times on the SAL store circuit board alone. The mistake is the series insertion of a diode between the output of one gate and the input to the next gate.

Design information published by Texas Instruments states that the maximum output voltage from a component with a logical "zero" output will be 0.4 volts. The maximum gate input voltage which will be recognized as a "zero" is 0.8 volts. Thus, the logic family has a guaranteed D.C. noise immunity of 0.4 volts, the difference between the "zero" outputs and inputs. Therefore, for the circuit of Fig. 3 to work reliably, the maximum acceptable forward voltage drop of the diode would be 0.4 volts.

Figure 3 shows both why typical circuits will work, at least at room temperature, and why circuits using worst case components will not work, particularly at the temperature extreme of -54°C. When the overall D.C. margin becomes negative, the circuit will not operate properly.

Figure 4 is a simplified schematic of another SAL circuit which violates the design rules for "zero" propagation. In this circuit, not only must the forward voltage drop of diode CR1 be taken into account, but also the collector-emitter saturation voltage of transistor Q1, typically 0.2 volts. The added 0.2 volt drop uses up whatever operating margin existed in the prior circuit of Fig. 3. For the circuit of Fig. 4 to operate at the temperature extreme of -54°C, components which are better than typical have to be selected.

The marginal performance of Fig. 4's circuit is illustrated by the waveforms of Fig. 5 which were obtained from a production model of the AN/UPA-60

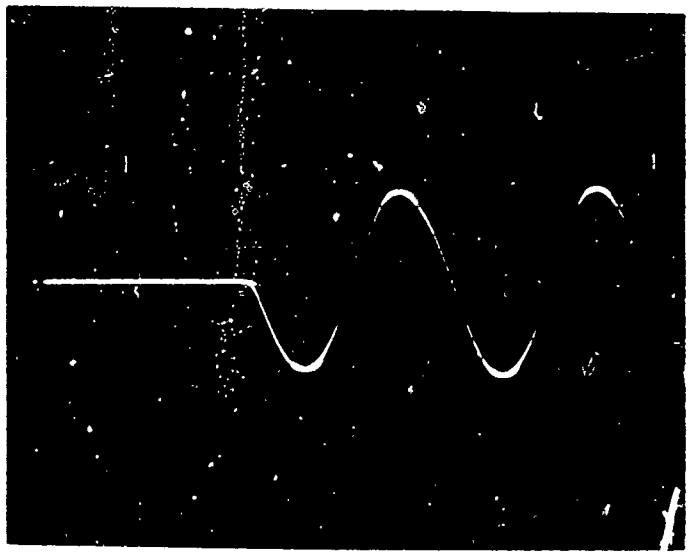
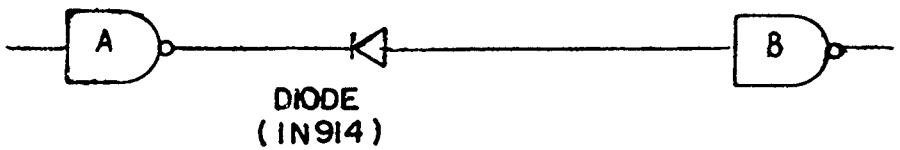


Fig. 1 - Existing SAL clock circuit output at "0" NM system range horizontal axis = 1 $\mu$s/Div.



Fig. 2 - Existing SAL clock circuit output at 200 NM system range horizontal axis = 1 $\mu$s/Div.




| TYPICAL | | WORST CASE | |
|---|---|---|---|
| LOGIC "0" OUT (GATE A) | =0.2V | LOGIC "0" OUT (GATE A) | =0.4V |
| DIODE VOLTAGE | =0.6V | DIODE VOLTAGE (-54°C) | = 0.7V (1.3V) |
| TOTAL "0" IN | 0.8V | TOTAL "0" IN (-54°C) | 1.1 V (1.7V) |
| LOGIC "0" IN (GATE A) | =1.4V | LOGIC "0" IN (GATE A) | =0.8V |
| D.C. MARGIN | =0.6V | D.C. MARGIN | =0.3V (-0.9V) |

Fig. 3 - TTL "0" propagation

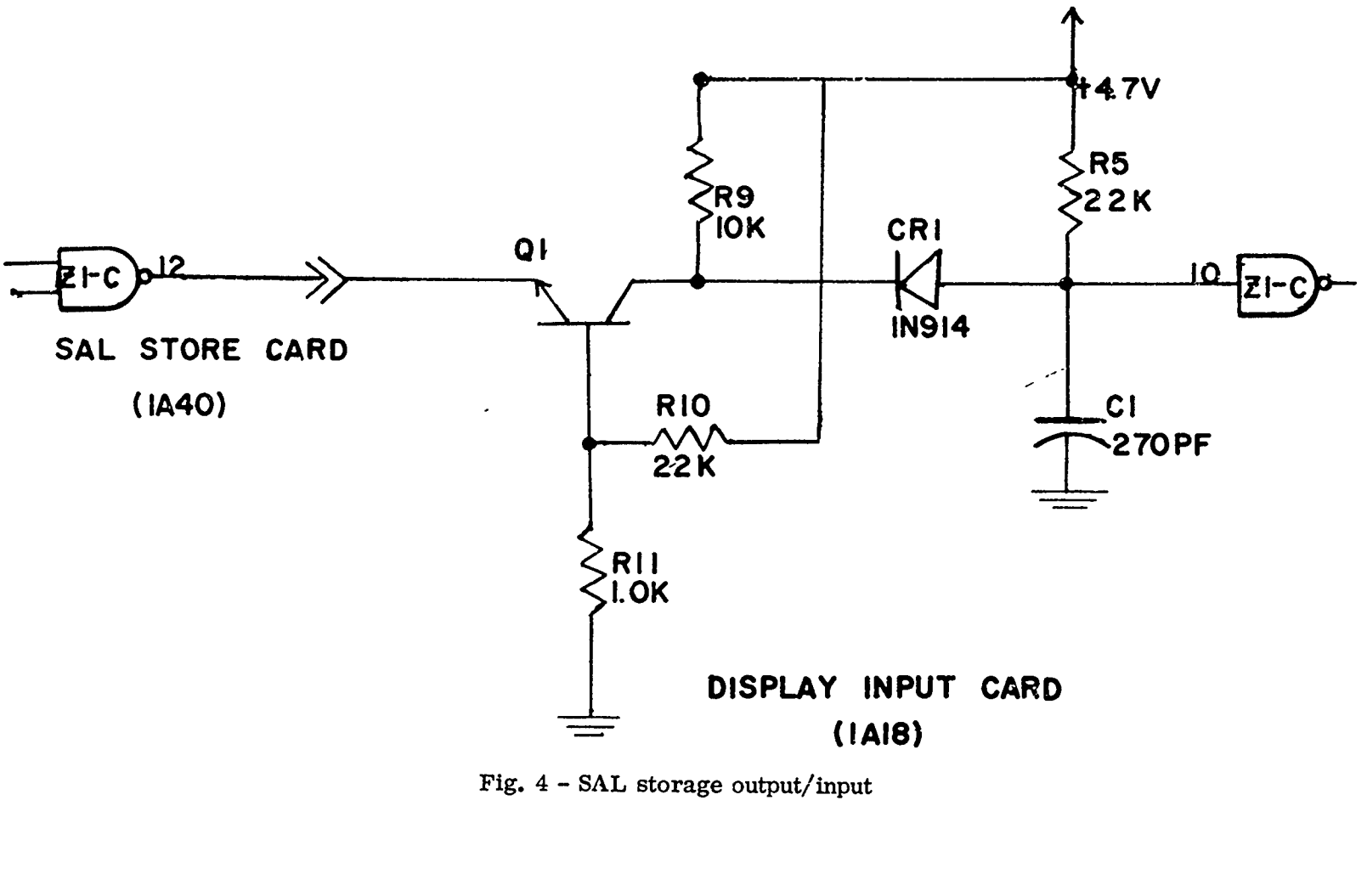



Fig. 4 - SAL storage output/input


Fig. 5 - SAL Storage Output/Input Waveforms

Top Trace - 1A40Z1C Output

Bottom Trace - 1A18Z1C Output

Vertical - 5V/Div

Horizontal - 1 μs/Div

decoder. The top trace is the inverted output from gate Z1C on the SAL store circuit board. The bottom trace is the output waveform from gate Z1C on the display input printed circuit card. The propagation delay shown, 0.5 microseconds, is far in excess of what is normally expected from components whose nominal turn-on delays added together is 0.15 microseconds; and is a result of marginal propagation characteristics.

Some of the design problems, the oscillator frequency differences and the excessive propagation delay in the circuit of Fig. 4, do cause noticeable operating problems for SAL parity. The primary problem is the creation of dead zones throughout the target display range. Within the dead zones, parity cannot be obtained, so there will be no parity display. When target range is changed slightly, parity is once again displayed. The dead zones occur periodically throughout the range, on a one-for-one basis with the register clock. The size of the dead zone is determined by the pulse widths of incoming signals and the range of the signal. Table 1 gives typical values measured with a production AN/UPA-69 decoder set up for operation in the NRL IFF system, a normal register clock period of 5.3 microseconds.

| | 2 NM Range | 200 NM Range |
|---|---|---|
| Pulse Width 0.35 μs | 0.95 μs | 0.27 μs |
| Pulse Width 0.45 μs | 0.80 μs | 0.23 μs |
| Pulse Width 0.55 μs | 0.70 μs | 0.21 μs |

TABLE 1 - SAL Parity Dead Zones

A secondary effect of the improper design technique is to make operation of the decoders at the temperature extremes a poor prospect. Also, field maintenance of the unit becomes difficult since repair technicians are not trained to recognize malfunctions caused by bad design rather than actual component failure.

## DESIGN OBJECTIVES

The identification of problem areas and inherent design flaws in the SAL Store circuit board led to a decision to attempt correction of the SAL parity

function by designing a replacement circuit board. A new SAL Store circuit board would replace the existing board on a one-for-one basis without any other modification to the equipment. In this manner, retrofit of all existing decoders, both the AN/UPA-59 and AN/UPA-60 would be possible in the field.

A set of design objectives to fulfill this task were drawn up. These objectives were:

1. The SAL memory would need to accommodate any length receiver gate without adjustments.

2. Readout of SAL data from the memory device should be non-destructive during successive parity mode interrogations.

3. The SAL memory should store the results of more than the latest Mode C interrogation. The first feasibility board should also have available means to determine the optimum number of stored interrogation results and the criteria for using the stored information.

4. Worst case design techniques would be used exclusively during design to insure operation under all environmental conditions.

5. The new circuit board should be totally interchangeable with the existing board, with no changes, either wiring or circuitry permitted in the basic decoder.

The preliminary design analysis showed that the use of shift registers to perform the actual memory function was still preferable over other techniques such as random-access memory circuits or content-addressable memory circuits. This decision was reached on the basis of size, cost, and ease of handling.

## USE OF THE RUBBER SHIFT REGISTER

As pointed out in a prior section of this report, one of the major problems with the SAL store printed circuit board was its inability to cope with variable PRFs and receiver gate periods. A general way of stating the problem is that data is loaded into the shift register beginning with the interrogation, or range zero ($R_O$) time, and is to continue until the end of the receiver gate. However, the end time of the gate is not known in advance, i.e., until it occurs, so that the data loaded into the register has in essence a variable length.

The function performed on the SAL store circuit board is that of range correlation, comparing the results of two or more events, always beginning with the $R_O$ time. This demands that data read out from the register be synchronous relative to $R_O$; the first data bit loaded into the register memory must be the first data bit read out regardless of the actual length of the data words. Therefore, the register memory circuitry has to adjust itself by some means to handle the variable length data word.

Solid State Scientific, Inc., has developed under contract from NRL a complementary MOS integrated circuit which fulfills the requirement for a variable-word-length register memory device. This component, called the rubber shift register, is a true variable-length shift register which automatically adjusts its length to that required by the incoming data word. The basic integrated circuit is that of a 64 bit register, a 64 bit counter, and associated control logic. The circuit has nine input/output lines, seven of which are needed to achieve variable-length operation. The circuit was designed so that any number of the basic 64 bit registers could be series connected giving whatever length register is needed for a specific application. Series connection results in a longer register which can effectively be treated as a single component, as control of operation is still maintained by the seven input/output lines of the basic circuit.

The 64 bit shift register has been divided into discrete steps of 16 bits each. Data output from the circuit is taken from one of the discrete steps as determined by the counter and internal logic. Although the register itself is broken into discrete steps of 16 bits, the integrated circuit has clock-control outputs so that, in the application of the circuit, it may still be treated as a totally variable-length register.

Operation of the rubber shift register can be explained with the aid of Fig. 6, the input/output diagram of the basic component. Operation of the circuit begins with the application of a single pulse to the START input line. Simultaneously with the application of the START pulse, the clock is started. Data is then accepted by the register at DATA INPUT and shifted through by the clock in normal shift register fashion. When the input data word is finished, a single pulse is applied to the STOP input line, which tells the register that the input word has ended.

Because the shift register is grouped into discrete 16 bit steps, the clock continues to shift data through the register until the first data input bit has reached a 16 bit multiple. At this time, a pulse is put out on the CLOCK OVERRIDE line which then stops the clock by external circuitry. During the time interval between the STOP pulse and the CLOCK OVERRIDE pulse the DATA INPUT is turned off internally, preventing invalid data from being loaded into the register.

The discrete 16 bit multiples are output tap positions from the register. Simultaneously with the appearance of the CLOCK OVERRIDE signal, flip-flops internal to the integrated circuit are set, selecting the register tap position used for data readout upon application of the next START pulse. In this way, the register has adapted itself to the actual length of the incoming data word.

Series operation of multiple rubber shift registers is obtained by the proper interconnection of the individual circuits. The DATA OUT from one circuit is fed to DATA IN of the next circuit in the chain. Likewise, the PROGRAM ACTIVATE from one circuit is connected to the START input of the next circuit in

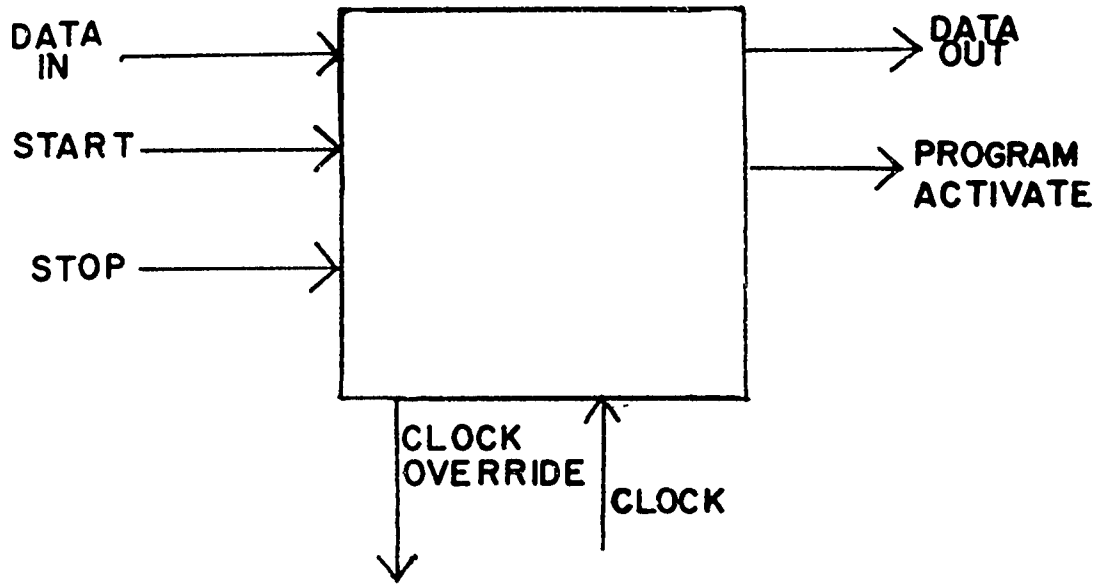



Fig. 6 - Rubber shift register inputs/output

series. The STOP inputs from all circuits in the chain are connected together in parallel as are all CLOCK inputs. The CLOCK OVERRIDE from the first circuit in the series is used to turn the clock off.

The PROGRAM ACTIVATE is initiated by the sixty-fourth clock pulse after the START pulse has been received. Since the PROGRAM ACTIVATE of one circuit is the START to the next circuit, the original START pulse is propagated through the series, but with a time delay equal to 64 clock periods for each prior circuit in series. It is by use of the PROGRAM ACTIVATE signal that responsibility for selection of the output tap for data read out is transferred from one circuit to the next circuit in the string.

Visualization of series operation can be aided by remembering that for each individual circuit only one of three possible conditions can exist. These conditions are:

a. The circuit has received a START (Program Activate from the prior circuit), there has not been a PROGRAM ACTIVATE output; thus upon receipt of the STOP signal the circuit decermines which output tap to select.

b. The circuit has received a START and it has produced a PROGRAM ACTIVATE; thus upon receipt of the STOP signal the output tap is set to the sixty-fourth bit of the register, keeping its full length in the overall chain.

c. The circuit has <u>not</u> received a START which also means that there could not have been a PROGRAM ACTIVATE output; thus upon receipt of the STOP signal the output tap is set to bypass all data directly from input to output, bypassing the entire register.

Typical series operation of several circuits will have the first circuits in series at their full length of 64 bits per circuit while the last circuits in series will bypass data directly from input to output. Only one circuit in the entire series string will need to determine exactly where the output tap is placed.

NEW SAL STORE - BLOCK DIAGRAM

A simplified block diagram of the new SAL store circuit board is presented in Fig. 7. The heart of this new circuit board is the three blocks of series-connected rubber register circuits, identified on the figure as Rubber Shift Registers 1, 2, and 3. Each of the register blocks contains eight rubber shift registers giving a grand total of 512 bits of storage in each block. It must be noted that 512 bits per register does not fulfill the specification requirement for range resolution of 0.4 nautical miles, as the actual granularity will be 0.69 nautical miles. However, this is still a little bit better than the original SAL Store board which used only 500 bits, giving range resolution of 0.70 nautical miles.

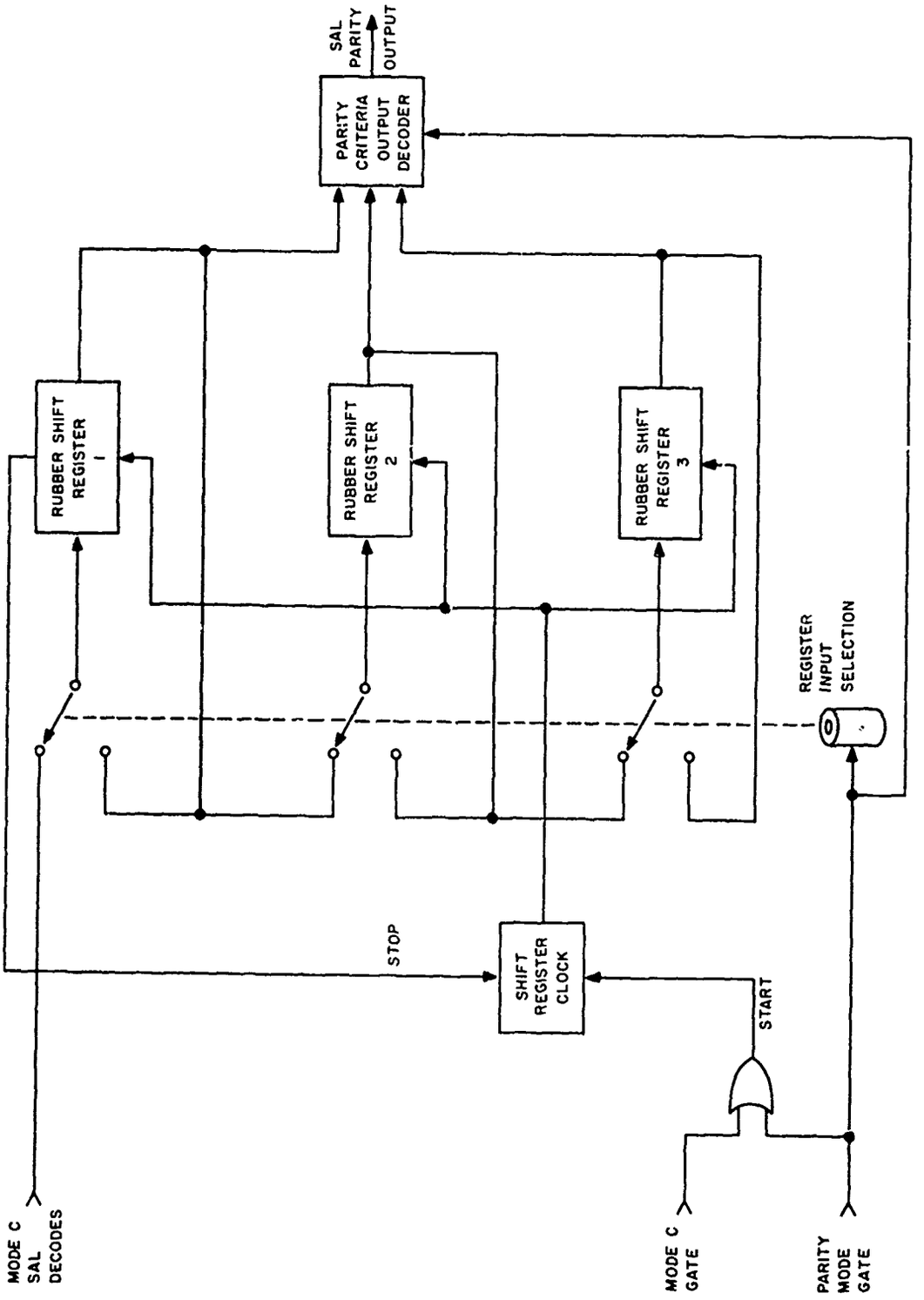



Fig. 7 - New SAL store circuit board block diagram

The primary reasons for not fulfilling this point of the specification were cost and printed board size. The rubber register circuits, because they were not in volume production, were quite costly. Completely meeting this requirement would have required an approximate doubling of the number of storage bits necessary. The decision not to fulfill this requirement, however, is justifiable on the basis of observed performance of the existing SAL Store board. Excessive range bin size would have shown up as false SAL parity decodes, both on targets and as fruit. This is exactly contrary to the previously noted problems with the existing circuitry.

The three register blocks each form an independent storage register, storing the SAL results of a separate Mode C interrogation. During a Mode C receiver gate period, the data currently being received is loaded into register 1. The data which had been in register 1 is being read out during this time and loaded into register 2. In a similar manner, the data which was in register 2 is transferred to register 3. The data which was stored in register 3 is lost. The overall result is that the SAL results of the last three Mode C interrogations are independently stored and available for SAL parity determination.

The data stored in the storage register is recirculated during the parity mode interrogations. The output from register 1 is fed both to the SAL parity decoder and also back to the input of register 1. The outputs of registers 2 and 3 are handled in an identical manner. As a result, the SAL data stored from the last three Mode C interrogations is not lost on the first parity mode interrogation, but is available for as many parity mode interrogations as may occur prior to the next Mode C interrogation.

Using three storage registers and recirculating the data when needed eliminates any apparent effect of interrogation interlace patterns upon the actual SAL parity display. This fixes the second major problem noted in the present SAL Store circuit board, that of inability to handle typical system interrogation sequences.

The first major problem of the present SAL Store circuit board, that of inability to handle varying interrogation PRFs and receiver gate periods, is corrected by the inherent characteristics of the rubber shift registers. The receiver gates, either Mode C or parity mode, form the Start and Stop pulses for controlling register operation. The leading edge of the gate is the Start pulse while the trailing edge is the Stop pulse. The range clock oscillator is also started with the leading edge of the gate, and continues until the clock Override signal is produced from register 1.

The third major problem in the present SAL Store circuit board, inherent electrical design flaws, was corrected in the detailed electrical design of the replacement board.

The SAL parity decoder block diagram (Fig. 7) can be set to make best use of the data stored in the three registers. Since the SAL results of the three Mode C interrogations are stored, the decoder can make decisions to either maximize the display of SAL parity, at the expense of possible fruit parity displays, or to essentially eliminate any chance of a false parity display. This is accomplished by setting a SAL parity decoding criteria. Typical criteria would be 1 out of 3, 2 out of 3, or even 3 out of 3; meaning that any number of SAL decodes within the last three Mode C interrogations can be sufficient to display parity, even if the latest Mode C interrogation was not decoded correctly.

## RUBBER SHIFT REGISTER PACKAGES

Implementation of the preliminary design for the new SAL Store circuit board required the use of twenty-four rubber shift register integrated circuits. Solid State Scientific, Inc., the manufacturer of the semiconductor devices, normally mounts the circuit chips into a 3/8" square flat pack. Because the very nature of this project was to replace SAL Store circuit boards on a one-for-one basis, all circuitry required would have to fit on a single board, identical to the existing board. The present board is approximately 4-1/2 inches square, although the usable area is reduced a small amount by the circuit board extractor and clearance for the card guides. It was obvious that using discrete rubber shift registers, each in its own package, was incompatible with printed circuit board size constraints.

It was decided to have a special package made, interconnecting numbers of the integrated circuit chips at the chip level, in order to reduce the overall size. Since the rubber register circuits were being used in three groups of eight series-connected circuits, it was decided to have the special package contain eight series-connected chips and use three of the special packages on the final board.

NRL contracted with Optimax, Inc., for design and construction of the special circuit module package. The circuit modules received on the contract each measured 1.1 inches square. The integrated circuit chips were mounted to an alumina substrate approximately 1 inch square. Once the chips were mounted to the substrate, the actual connection was by wire bonding between the chips and a conductive pattern which had been previously printed on the substrate. The conductive pattern then performed the actual interconnection of the circuits.

The substrate with all the integrated circuit chips attached and bonded, shown in the photograph of Fig. 8, is then mounted to a header. A cover is then soldered to the header assembly giving a final package which is hermetically sealed.

Due to the inherent design of the rubber shift register circuit, the final special package, other than the actual number of storage bits, is electrically indistinguishable from the basic rubber shift register. As such, it is very possible that other uses for the final circuit may be found.

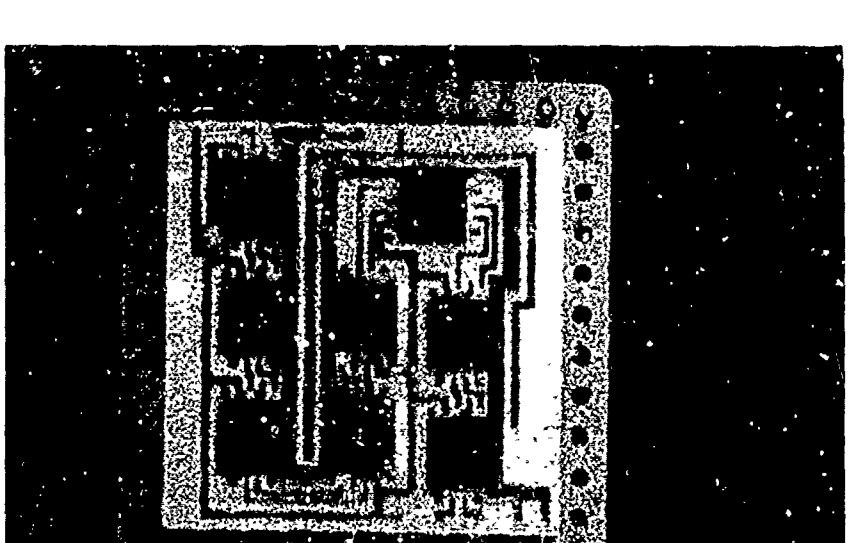


Fig. 8 - Optimax P-1610 circuit module
(Internal View)

There was one unanticipated advantage to using the Optimax circuit module. The conductive patterns on the substrate, with multiple levels of metallization for the grounds and voltage distribution buses, acted as an extremely good high-frequency decoupling capacitor, permitting circuit operation with higher noise immunities than were noted on the first breadboards.

## FINAL ELECTRICAL DESIGN

The full schematic diagram of the finished SAL Store circuit board is shown in Fig. 9. All circuits were designed such that complete electrical interchangeability with the present circuit board was maintained.

One point, that should be made, concerns the use of available power supply voltages to perform circuit functions. The rubber shift register circuits as pointed out previously are made by the complementary MOS process. This process gives circuits which inherently have a large immunity to supply voltage variations. Present day technology produces complementary MOS circuits which are able to operate with supply voltages between 3 to 15 volts. However, the rubber shift register chips used on the feasibility circuit board were not made with the latest production processes and would operate reliably only with supply voltages down to 6 volts. Therefore, it was not possible to operate the rubber registers off of the + 4.7 supply and interface directly into TTL logic. Instead, the -12 volt supply was used to operate the rubber shift registers, and other C MOS gates requiring a large number of interface circuits between the TTL voltage levels and complementary MOS voltage levels. The circuitry of transistors Q4 through Q11 could have been essentially eliminated if this interfacing had not been required.

Operation of the new Sal Store card begins with the R-S type flip-flop gates of Z1B and Z2A. Application of either the Mode C gate or a parity gate to the flip-flop starts the clock oscillator composed of transistors Q1 through Q3. The circuitry of the oscillator is essentially identical with that of the prior circuit board. The changes made were the addition of S1 and multiple timing capacitors C4 through C8 and improvement in the supply voltage decoupling to eliminate the frequency shifting problem previously described. The addition of the switch and multiple capacitors was made to allow evaluation of the effect of various range bin sizes upon overall performance and would not be included in a final design.

The output from the clock oscillator is fed through logic elements Z3A, Z1D, and Z5 to standardize the clock pulse shape. The proper voltage levels for the clock pulses are then generated by transistors Q8 and Q9 and networks Z12 and Z13. These outputs drive the rubber shift registers directly.

The START pulse for the rubber shift registers is obtained from the leading edge of the clock oscillator flip-flop gate acting through transistor Q6. The STOP pulse for the rubber shift registers is obtained from the trailing edge of either the Mode C gate or the parity gate, gate Z2B performing the OR function, as detected by transistor Q5.

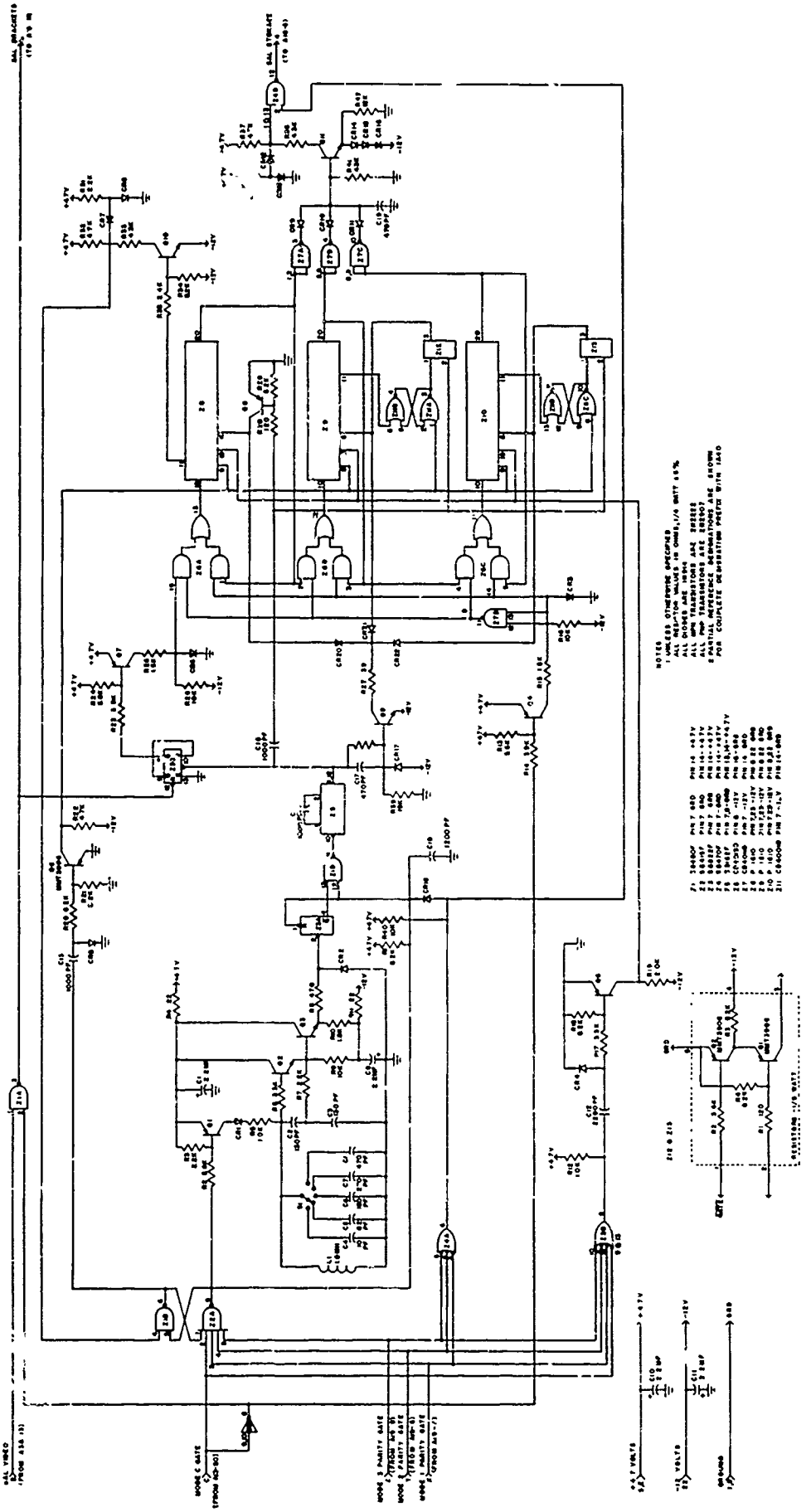


Fig. 9 – SAL storage card (1A40) for AN/UPA-59/60 decoders
(Proposed Working Mod.)

SAL video, the Mode C SAL decodes, is gated through Z1A by the Mode C gate. The output from Z1A is fed to flip-flop Z3B, to insure its time duration is sufficient to overlap the time of a clock pulse and thus be read into the first rubber shift register. The interface of data input to the first rubber shift register is performed by transistor Q7.

Gates Z6A, B, and C perform the input selection to the three rubber shift register blocks. This determines either if data already in the rubber shift registers will be recirculated, as during the parity mode, or read in new, during the Mode C gate time.

The previous discussion of the operation of the rubber shift register pointed out that, as a component, it performs its own logic for synchronization. However, its synchronization is in the form of a pulse to stop application of clock pulses to the circuit. The gates of Z11 form two R-S flip-flops which gate the application of clock pulses to the second and third rubber shift register blocks. The clock override output from the first rubber shift register block is fed to the interface circuitry of transistor Q10 which in turn rests the Z1B-Z2A input flip-flop.

Logic gates Z7A, B, and C. complementary MOS gates, are the output criteria decoding gates. Figure 9 shows these gates set up for a one-out-of three criteria, although as noted previously, other output criteria are possible. Diodes CR9 through CR10 and transistor Q11 perform an OR function on the output criteria decoding gates. Transistor Q11 also accomplishes the voltage level interfacing to the TTL output gate, Z4B.

The second input to NAND gate Z4B is the output of gate Z4A, which performs an OR function on the individual Mode 1, Mode 2, and Mode 3 parity gate inputs. The output from gate Z4B is what is ultimately fed through the remainder of the decoder's circuitry to become the actual SAL parity display.

A photograph of the actual printed circuit card built on this project is shown in Fig. 10. The three special rubber shift register packages built for this project, the Optimax P-1610 modules, are in the upper left-hand corner of the circuit board. The clock oscillator circuitry is in the upper right-hand corner of the circuit board. The area occupied by the clock oscillator has been isolated from the remainder of the circuitry by a ground pattern.

From examination of Fig. 10, it can readily be seen that the amount of interfacing circuitry required between the complementary MOS circuits and the TTL circuits was quite extensive. This voltage level interfacing occupied almost 1/3 of the total board area and accounted for over 1/2 of the number of individual piece parts. If rubber registers had been obtained that could have worked from the + 4.7 volt supply, the final complexity would have been greatly reduced. This can not be too strongly recommended for an actual production version of this circuit board.

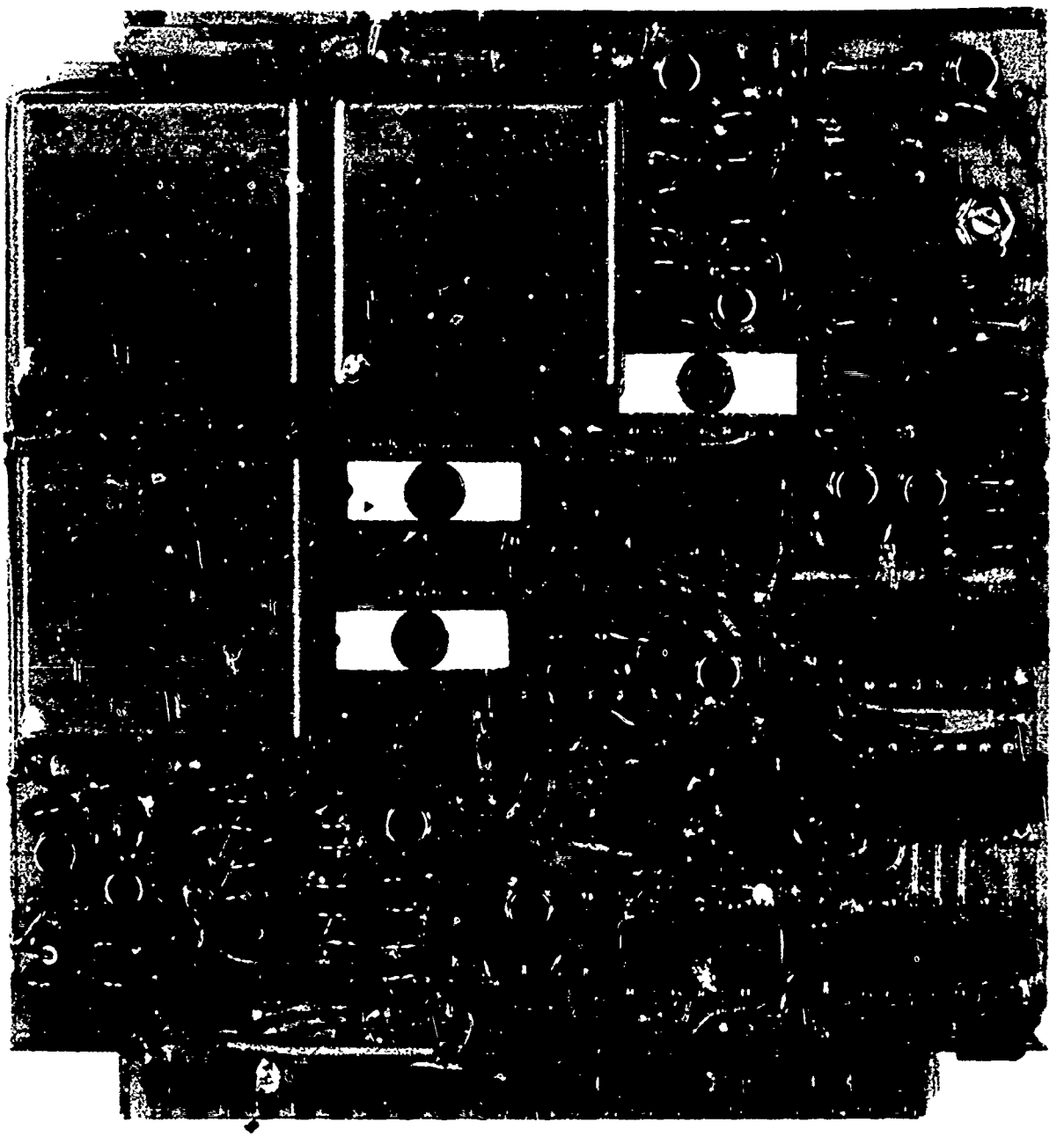


Fig. 10 - Feasibility model printed board for SAL parity on AN/UPA-59/60 IFF decoder

## SAL STORE CIRCUIT BOARD PERFORMANCE

The new SAL Store printed circuit board was tested extensively in an AN/UPA-60 decoder group operating in NRL's IFF ground system. The testing was done to determine not only what the circuitry functioned correctly as designed, but also to determine somewhat if the original specifications applied to the SAL parity function in the decoder were realistic.

The nature of the SAL parity function makes the collection of actual numerical data extremely difficult. If one were to consider the old SAL Store circuit board, the actual numerical specification values were somewhat complied with, although the board would still not work properly in a live, operating IFF system.

Also, the original specification could be looked at from a viewpoint of restricting the flow of information through the decoder. The range bin size was very small although there was no published data to indicate what bin size was desirable. There also was no known reason to restrict parity determination to the results of only one interrogation, either parity or Mode C.

Testing of the finished board, therefore, was primarily concerned with what would be the adverse effect of maximizing information throughput. The range bin size was set to the maximum allowable by the range clock oscillator, 0.69 nautical miles, compared with the specification value of 0.40 nautical miles. The output decoding criteria was set for the one-out-of three criteria, maximizing the adverse effects of false decodes.

The data obtained on the final board, set up for maximum information flow, is contained in a series of eight PPI photographs, Figures 11 through 18. These photographs are side by side comparisons of the new SAL Store circuit board compared to the old SAL Store board. These photographs are of both short and long operating range situations, with and without defruiting of decoder input video.

The ground system operating parameters for these photographs were an interlace sequence count set to four, system range gate set to 225 nautical miles, system operating PRF of 280, and an antenna rotation rate of 6 RPM. The typical measured fruit density observed at the NRL ground site is 13,000 bracket decodes per second.

Figures 11 through 14 have the PPI set for a relatively short range display with a radius of approximately 60 nautical miles. The decoder group was set to passively decode Mode 3, Code 2100. The SAL switches were set to an upper limit of 32,000 feet and a lower limit of 30,000 feet, giving an effective SAL layer of 2,000 feet. This presents close to a worst case since there is less tolerance for Mode C decoding mistakes.

Figures 15 through 18 have the PPI set for a long range display equal to the system range of approximately 225 nautical miles. The decoder was still set for a passive decode of Mode 3, Code 2100. This code was chosen to obtain a maximum number of targets. The upper limit of the SAL layer was set to 45,000 feet with

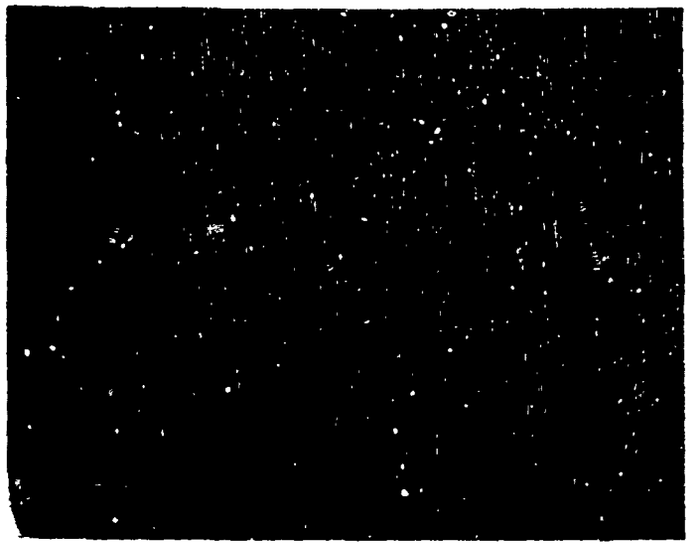


Fig. 11 - Present SAL board undefruited
video 60 NM range



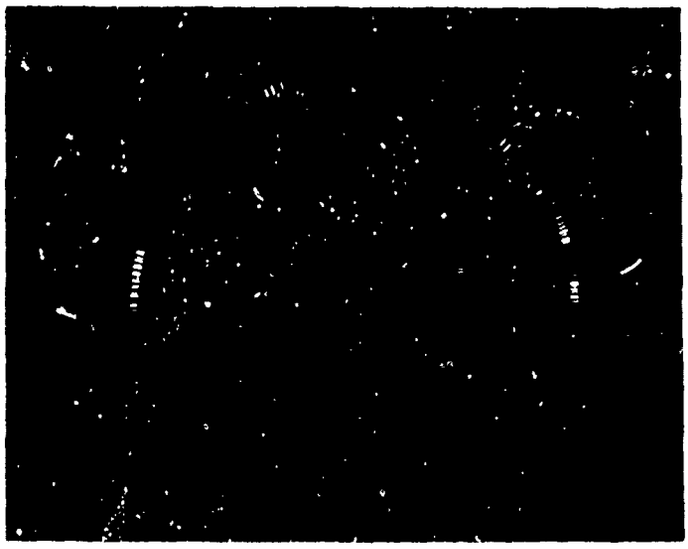


Fig. 12 - New SAL board undefruited
video 60 NM range

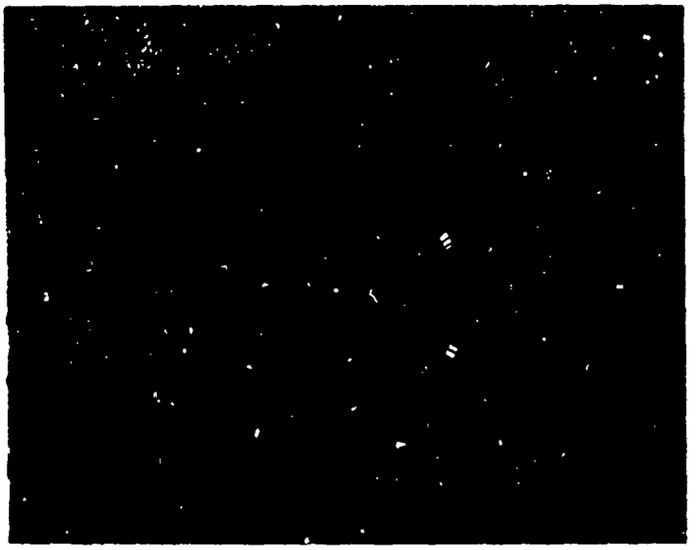


Fig 13 - Present SAL board defruited
video 60 NM range



Fig. 14 - New SAL board defruited
video 60 NM range

Fig. 15 - Present SAL board undefruited video 200 NM range



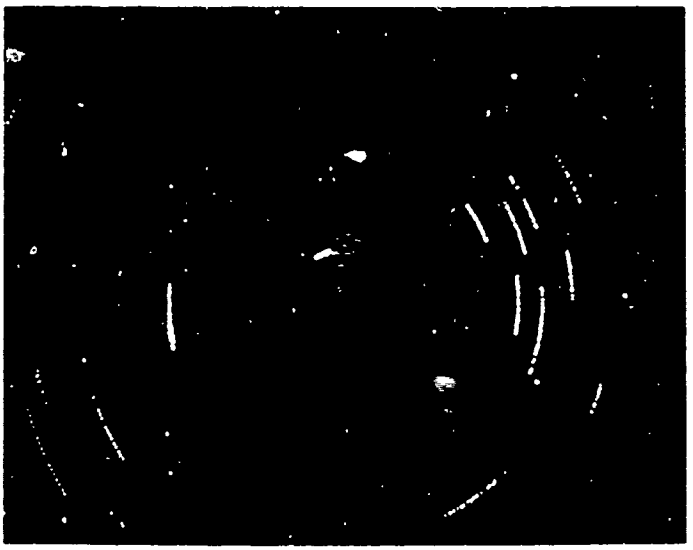


Fig. 16 - New SAL board undefruited video 200 NM range

Fig. 17 - Present SAL board defruited
video 200 NM range



Fig. 18 - New SAL board defruited
video 200 NM range

a lower limit of 5,000 feet. This reduces the effect of improper decoding of the Mode C responses and at the same time maximizes the chance of SAL parity disp'ay mistake, i.e., display of fruit.

SAL parity display mistakes, extraneous fruit, is shown as a stretched fruit pulse in all the photographs. As can be seen from the photographs, even maximizing information flow through the new SAL circuitry does not give an excessive number of false displays. This is particularly true of normal IFF systems which use a defruiter of some type in the system.

The other observation which can be drawn from the photographs is that the quality of the display obtained from the new SAL Store circuit board is superior to that of the old circuit board.

The new SAL Store circuit board was also tested for its ability to handle varying PRFs and receiver gate periods without any readjustment of either the circuit board itself or any front panel controls. The results from this test were as expected, the new SAL Store board was able to accommodate all PRF and receiver gate changes without any control changes. The old SAL Store card was reinserted in the decoder and it was noted that no parity display whatsoever was obtained.

## CONCLUSIONS

This project has proven the feasibility of modifying the AN/UPA-59/60 IFF decoders for proper operation of the SAL parity display function. This modification consists of a simple printed circuit board replacement for the existing SAL Store circuit card in the decoders. The new SAL Store circuit board which has been covered in this report is one such approach to the problem and was found to eliminate all prior observed problem areas.

The present specification for SAL parity operation was found to be not sufficient in that it is overly restrictive in some areas and does not properly define what SAL parity operation is and under what conditions it must work. Also, the original contractor for the AN/UPA-59/60 decoders is somewhat responsible for improper operation of the SAL parity function by use of improper design practices and insufficient thought to system operation.

The rubber shift register integrated circuit has been proven to be an extremely useful component for IFF system and subsystem design. This circuit, more than any other component, is responsible for being able to construct the feasibility model circuit boards for modifying existing IFF decoders.

It is recommended that a program to retrofit all existing decoders for proper operation of SAL parity be initiated. Such a program would have two advantages. The first is that maximum usefulness of the decoders would be obtained,

the second is that it would permit production quantities of the rubber shift register integrated circuit to be built, reducing its cost, and thereby permitting its use in more applications.

ACKNOWLEDGEMENTS

The author wishes to acknowledge the splendid assistance and cooperation provided by Messrs. Eugene George and Ron Fulton in testing operation of the new SAL Store circuit board in the NRL ground system and Mr. William Beiles who performed the printed circuit board layout for the finished model.